Memory Device

The present invention relates to a memory device for data storage and in particular the invention relates to a memory device which makes use of the piezoelectric effect.

Ferroelectric materials, as a sub-set of piezoelectric materials, can exhibit a non-volatile, bi-stable internal polarisation. The state of polarisation is established by the application of a voltage between opposing surfaces of the material. Having applied a sufficiently large voltage to internally polarise the material, it ought subsequently to be possible to determine the direction of polarisation - which can be used as a binary indicator, whereby the material can act as a data storage medium. However, a problem arises in that the data read operation is destructive of the data. Specifically, the read operation would consist of applying a voltage to set the polarisation in a specified direction. If the polarisation is already in that direction no charge exchange is required. However, if the polarisation is in the opposite direction a relatively large amount of charge exchange is required to establish the specified direction of polarisation. Thus, the previous direction of polarisation can be judged according to the high or low (zero) level of charge exchange required to establish the specified polarisation.

It is an object of the present invention to provide a memory device which makes use of the internal polarisation of a ferroelectric material for data storage and in which a non-destructive data read operation can be undertaken. It is another object of the present invention to provide a method of data storage and retrieval which makes use of the internal polarisation of a ferroelectric material and in which a non-destructive data read operation can be undertaken.

According to a first aspect of the present invention there is provided a memory device comprising a layer of piezoelectric material and a layer of ferroelectric material clamped

together such that a voltage applied to one layer results in a voltage being generated across the other layer. Preferably, the piezoelectric material is implemented as a ferroelectric material.

According to a second aspect of the present invention there is provided a method of data storage and retrieval comprising the steps of: providing a layer of ferroelectric material, providing a layer of piezoelectric material, clamping the two layers together, storing data by internally polarising the ferroelectric material in one of two stable directions in accordance with the data to be stored, and retrieving stored data by applying a non-polarising voltage to one layer and detecting a resultant voltage from the other layer. Preferably, the step of providing a layer of piezoelectric material comprises the step of providing a ferroelectric material as that piezoelectric material.

Embodiments of the present invention will now be described in more detail, by way of further example only and with reference to the accompanying drawings, in which:-

Figure 1 illustrates the principle of operation of a piezoelectric device which acts as a voltage amplifier;

Figure 2 is a diagrammatic representation of data storage modes in a memory device according to one embodiment of the present invention;

Figure 3 is a diagrammatic representation of a multi-cell memory device according to another embodiment of the present invention;

Figure 4 illustrates a data read operation for a single cell memory device; and

Figure 5 illustrates the application of a conventional addressing scheme to a matrix memory device according to the present invention.

A description of the principle of operation of a piezoelectric device acting as a voltage amplifier will now be given, with reference to figure 1. As illustrated in figure 1, two layers (1, 2) of piezoelectric material are confined between two clamping members (3, 4). The voltage associated with the first layer (1) of piezoelectric material is referenced as V_1, it's

thickness as d_1 and its inherent characteristics as ε_{r1} and $d_{33,1}$. Similarly, the voltage associated with the second layer (2) of piezoelectric material is referenced as V_2, it's thickness as d_2 and its inherent characteristics as ε_{r2} and $d_{33,2}$. Ideally,

$$\Delta d_i(E_i) \equiv d_i(E_i) - d_i(0) \approx d_{33,i} d_i(0) E_i \approx d_{33,i} V_i$$

Due to the external confinement of the layers, $\Sigma \Delta d_i = 0$ and hence:-

$$V_2 = \pm (d_{33,1}/d_{33,2}) V_1$$

where the signs correspond to the parallel and anti-parallel polarisation between layers 1 and 2.

The device illustrated in figure 1 may be referred to as a ferroelectric amplifier, ferroelectric and piezoelectric effects being considered to co-exist.

As already noted, a relatively large voltage is required to change the direction of polarisation of the ferroelectric materials. Applying a relatively small voltage will not change the direction of polarisation. Thus, in the device illustrated in figure 1 applying a small voltage V_1 will not change the polarisation of layer 1 but by reading the sign of the consequential output V_2 (the magnitude of which is sufficiently small so as not to change the direction of polarisation of layer 2) the parallel or anti-parallel polarisation directions of layers 1 and 2 is immediately, and non-destructively, detected. Thus, considering the polarisation direction of one of the layers as a reference and arranging for the polarisation direction of the other layer to be changed to represent a binary indicator, a non-volatile memory device is provided in which non-destructive reading of the binary indicator is performed simply by phase comparison of the input and output read voltages. An example of the thus described basic cell is illustrated in figure 2.

In figure 2, the polarisation of the lower layer is used as the reference and the polarisation of the upper layer is used for data storage. As illustrated, the parallel polarisation condition has been associated with binary "1", input and output voltages being out of phase,

and the anti-parallel polarisation condition is associated with binary "0", input and output voltages being in phase.

A particular advantage of the memory device according to the present invention is that it is not easily affected by external disturbance. The displacement involved in the read out is internal and relative. It can be considered analogous to the optical mode of phonons. External disturbance, eg vibrations, is similar to the acoustic mode and has very little impact on the output.

From the foregoing description it will be appreciated that one aspect of the present invention resides in the use of the piezoelectric effect to read data from a memory cell. Specifically, the so-called reference layer of figure 2 can be implemented as a piezoelectric layer rather than a ferroelectric layer. Applying a voltage to the piezoelectric layer causes a contraction or expansion of the piezoelectric layer and a resulting change in the ferroelectric layer, which change is detectably dependent upon the direction of polarisation of the ferroelectric material. This can be considered as an in-phase only version of the embodiment of figure 2. Further, although clamping of the layers has been illustrated in terms of a physical confinement (constant distance), clamping of the layers is also to be understood as subjecting them to a constant force (stress) - for example. The requirement is that the change in one layer should act upon the other layer and not be lost externally.

The operation of a single memory cell has been described with reference to figures 1 and 2. For practical use it is desirable to provide an array of many cells. Such an array can readily be provided in accordance with the present invention. The basic cell requires three electrodes. These are identified by reference numerals 5, 6 and 7 in figure 1. That is, voltage V_1 is applied between electrodes 5 and 6 and voltage V_2 is measured between electrodes 6 and 7. Although a common electrode 6 is illustrated, it would of course be feasible to use two respective separate electrodes, for the upper and lower layers, in place thereof. As shown in

figure 3, an array of cells is formed by providing a respective plurality of electrodes 5, 6 and 7. A plurality of elongate, parallel and spaced apart electrodes 5 are provided in one plane. A similar plurality of elongate, parallel and spaced apart electrodes 7 are provided in a parallel plane and a plurality of elongate, parallel and spaced apart electrodes 6 are provided in another parallel plane, between the other two planes. Further, the electrodes 5 and 7 are parallel to each other and vertically aligned whereas the electrodes 6 are perpendicular to electrodes 5 and 7. Individual memory cells are thus formed at each point of "intersection" or overlap of respective individual electrodes 5, 6 and 7.

As illustrated in figure 4, a comparator 8 is used to read each memory cell. Comparator 8 compares the sign, or phase, of the voltages V_1 and V_2 and the output can be taken directly as the binary value "1" or "0". It is a particular advantage of the present invention that the data content of the memory cell can be read using a simple comparator circuit.

The memory array explained with reference to figure 3, using a plurality of comparators as described with reference to figure 4, can be used to implement either an active or a passive matrix. Importantly, the resulting matrix can be addressed using conventional addressing techniques. The matrix connections for conventional addressing of a plurality of memory cells according to the present invention is depicted in figure 5.

The aforegoing description has been given by way of example only and it will be appreciated by a person skilled in the art that modifications can be made without departing from the scope of the present invention.